

GP 2812

TSMC 98-275



March 26, 1999

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
20 McIntosh Drive
Poughkeepsie, N.Y. 12603

Subject:

Serial No. 09/249,254 02/12/99

Y.S. Ho, J.Y. Chung, C.H. Chen,
H.J. Tao

METHOD OF MAKING A METAL-INSULATOR
METAL CAPACITOR IN THE CMOS PROCESS

Grp. Art Unit: 2812

RECEIVED
99 APR 1 PM 2:18
TECHNOLOGY CENTER 2800

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56. Copies of each document is included herewith.

U.S. Patent 5,037,772 to McDonald, "Method for Forming a
Polysilicon to Polysilicon Capacitor", describes a method where
a first polysilicon layer is initially deposited onto a layer
of field oxide. A dielectric is formed and then a second
polysilicon layer is deposited.

U.S. Patent 4,697,330 to Paterson et al, "Floating Gate Memory Process with Improved Dielectric", describes a method where the dielectric between the floating gate and the control gate, in an EEPROM or other floating gate memory is made by forming an oxide/nitride stack over the (first polysilicon) control gate.

U.S. Patent 5,338,701 to Hsu et al., "Method for Fabrication of W-Polycide-To-Poly Capacitors with High Linearity", describes a method of forming a polycide-to-polysilicon capacitor simultaneously with a CMOS device with polycide gate.

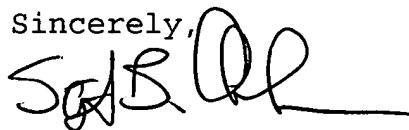
U.S. Patent 5,589,416 to Chittipeddi, "Process for Forming Integrated Capacitors", teaches fabrication of a metal-oxide-polysilicon capacitor.

U.S. Patent 5,554,558 to Hsu et al., "Method of Making High Precision W-Polycide-To-Poly Capacitors in Digital/Analog Process", discloses a very high integrity capacitor dielectric in a polysilicon to polysilicon or polysilicon to metal capacitor.

The following seven U.S. Patents disclose various methods of forming metal-insulator-metal capacitors:

1. U.S. Patent 5,576,240 to Radosevich et al., "Method for Making a Metal to Metal Capacitor".
2. U.S. Patent 5,654,581 to Radosevich et al., "Integrated Circuit Capacitor".
3. U.S. Patent 5,479,316 to Smrtic et al., "Integrated Circuit Metal-Oxide-Metal Capacitor and Method of Making Same".
4. U.S. Patent 5,708,559 to Brabazon et al., "Precision Analog Metal-Metal Capacitor".
5. U.S. Patent 5,406,447 to Miyazaki, "Capacitor Used in an Integrated Circuit and Comprising Opposing Electrodes Having Barrier Metal Films in Contact with a Dielectric Film".
6. U.S. Patent 5,741,721 to Stevens, "Method of Forming Capacitors and Interconnect Lines".
7. U.S. Patent 4,971,924 to Tigelaar et al., "Metal Plate Capacitor and Method for Making the Same".

Sincerely,

A handwritten signature in black ink, appearing to read "SBA", followed by a long horizontal flourish.

Stephen B. Ackerman,
Reg. No. 37661

INFORMATION DISCLOSURE CITATION
IN AN APPLICATION

TSMC-98-275

09/249,254

Applicant Y. S. Ho et al.

Filing Date 02/12/99

Group Art Unit 2812

(Use several sheets if necessary)

U. S. PATENT DOCUMENTS

EXAMINE PATENT & TRADEMARK OFFICE	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILED DATE IF APPROPRIATE
01 P E J C 61 MAR 28 1999	5037772	8/6/91	McDonald	437	52	12/13/89
	4697330	10/6/87	Paterson et al.	437	42	5/27/86
	5338701	8/16/94	Hsu et al.	437	60	11/3/93
	5589416	12/3/96	Chittipeddi	437	60	12/6/95
	5554558	9/10/96	Hsu et al.	437	60	2/13/95
	5576240	11/19/96	Radosevich et al.	437	60	12/9/94
	5654581	8/5/97	Radosevich et al.	257	534	6/6/95
	5479316	12/2/95	Smrtic et al.	361	322	8/24/93
	5708559	1/13/98	Brabazon et al.	361	313	10/27/95
	5406447	4/1/95	Miyazaki	301	313	12/29/92
	5741721	4/21/98	Stevens	437	60	4/12/96

FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
					YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

RECEIVED
99 APR - 1 P 12:18
TECHNOLOGY CENTER 2800

QIP E INFORM
MAR 29 1999
61
3
MARK OFFICE

Docket Number (Criminal)

Tsmc - 98-275

Application Number

09/249, 25.4

Applicant:

Y.S. Ho et al.

Filing Date

02/12/99

Group Art Unit

2812

[illegible][illegible][illegible]

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.